Application Note

LXT310/318 TO CS61310/18 REPLACEMENT GUIDE

1. INTRODUCTION

The purpose of this application note is to provide design suggestions and recommendations for customers wishing to replace Level One Long Haul Line Interface Units (LIUs) with the Cirrus Logic equivalents. Specifically, considerations for replacing the LXT310 T1 Long Haul LIU with the CS61310 are covered; as are considerations for replacing the LXT318 E1 Long Haul LIU with the CS61318. This document is intended to be used in conjuction with the CS61310 and CS61318 data sheets.

In short, only the resistors on the receive channel need to be changed if an LXT310 is to be replaced with a CS61310. Otherwise, all circuitry and all software remain the same. There are no changes that need to be performed if an LXT318 is to be replaced with a CS61318. Thus it is very easy to replace the LXT310/318 with Cirrus Logic's CS61310/18 equivalent parts.

While the required changes are minimal, users will gain additional functionality inherent to the Cirrus Logic Crystal® line of telecommunications ICs. These additional features include:

- Crystal-less jitter attenuation
- User programmable pulse shapes
- Network loopback signal generation and detection
- Line quality, LOS and AIS monitoring in all modes

If desired, users may make use of this functionality as detailed in Section 4, *Comparisons*.

The CS61310/18 are 5.0V devices available in both PLCC and PDIP package styles, and are released to high volume production. Customer Evaluation Kits are available for these devices, part number CDB61310/318. For in-depth details regarding theory of operation, please view the respective product data sheets.

Device #	Description	Replaces	Package	Power	Temp.
CS61310-IL	T1 LH LIU	LXT310PE	28-pin PLCC	5V	Industrial
CS61310-IP	T1 LH LIU	LXT310NE	28-pin PDIP	5V	Industrial
CS61318-IL	E1 LH LIU	LXT318PE	28-pin PLCC	5V	Industrial
CS61318-IP	E1 LH LIU	LXT318NE	28-pin PDIP	5V	Industrial

Table 1. Cirrus Replacements for Level One Long Haul LIUs

CIRRUS LOGIC®
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

2. BENEFITS OF FEATURES UNIQUE TO CIRRUS LOGIC

The additional functionality that a user gains by replacing the LXT310/318 with the CS61310/18 includes the following:

- Crystal-less Jitter Attenuation: This feature reduces system cost because the CS61310/18 were designed to meet stringent jitter attenuation specs without the expense of external circuitry.
- User Programmable Pulse Shapes: This feature allows the user to program the CS61310/18 to compensate for pulse degradation caused by non-standard cables, transformers, or protection circuitry. As a result, the customer saves the time and money associated with tweaking the analog hardware design to achieve T1/E1 pulse shape compliance. In some applications, this feature allows the user to reduce the T1/E1 pulse amplitude as a means to save power.
- Network Loopback Signal Generation and Detection (Loop Up/Loop Down): These features support enhanced link diagnostics and error detection without requiring human intervention at the far end.
- Line Quality, LOS and AIS Monitoring Available In All Modes: The CS61310/18's line quality monitor provides the highest line quality resolution of any LIU on the market. Consequently, the user has a much more accurate picture of the line condition. The user also has the flexibility of using either hardware or host mode to monitor the CS61310/18's LOS and AIS status.

3. FREQUENTLY ASKED QUESTIONS

- Is the CS61310 a drop-in replacement for the LXT310, requiring no circuit changes?

  ANSWER: The use of the CS61310 device in a previously-LXT310 socket requires only one change. The values of the transmit resistors should be changed to 9.1 Ω from the LXT310 requirement of 12.5 Ω. In applications where common mode noise is an issue, Cirrus recommends the addition of a 0.47 µF capacitor on the receive circuit (see CS61310 datasheet).

- Is the CS61318 a drop-in replacement for the LXT318, requiring no circuit changes?

  ANSWER: Yes! A CS61318 device can be used in an previously LXT318 socket with NO changes to the circuit. In applications where common mode noise is an issue, Cirrus recommends the addition of a 0.47 µF capacitor on the receive circuit (see CS61318 datasheet).

- Are there any software changes required when replacing the LXT310/318 with the CS61310/18?

  ANSWER: No! There are NO software changes required to use the CS61310/18 in the same manner as the Level One equivalents. However, the CS61310/18 do offer additional functionality, beyond the capabilities of the respective Level One devices. If the user wishes, they can modify their software to access the features unique to Crystal Long Haul LIUs.

4. COMPARISONS

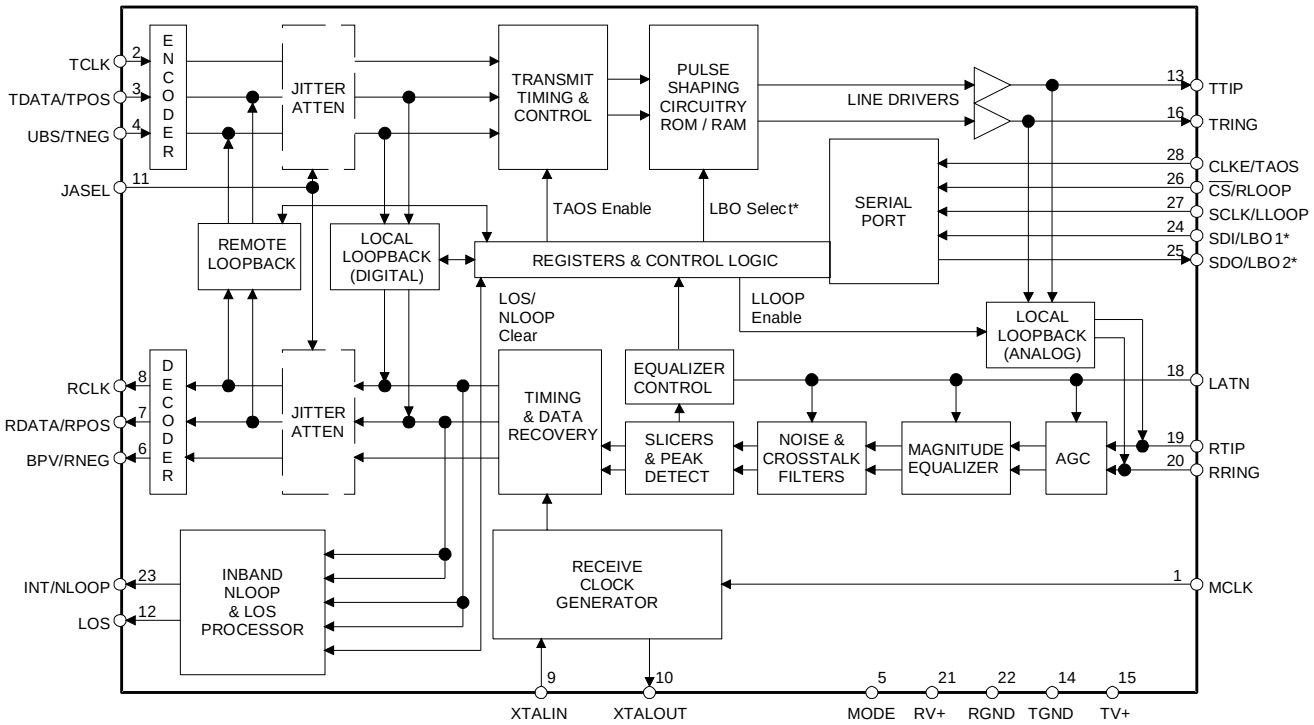
4.1 Block Diagram: CS61310/18 Shown

The functional blocks internal to the CS61310/18 are shown below in Figure 1.

4.2 Pinouts

The pinout of the CS61310 differs from that of the LXT310 by one pin, pin 17. The CS61310 data sheet refers to this pin as a "No Connect", while the data sheet for the LXT310 refers to this pin as "Equalizer Gain Limit". The LXT310 application drawings show this pin as connected to ground, which is an acceptable option for pin 17 of the CS61310.

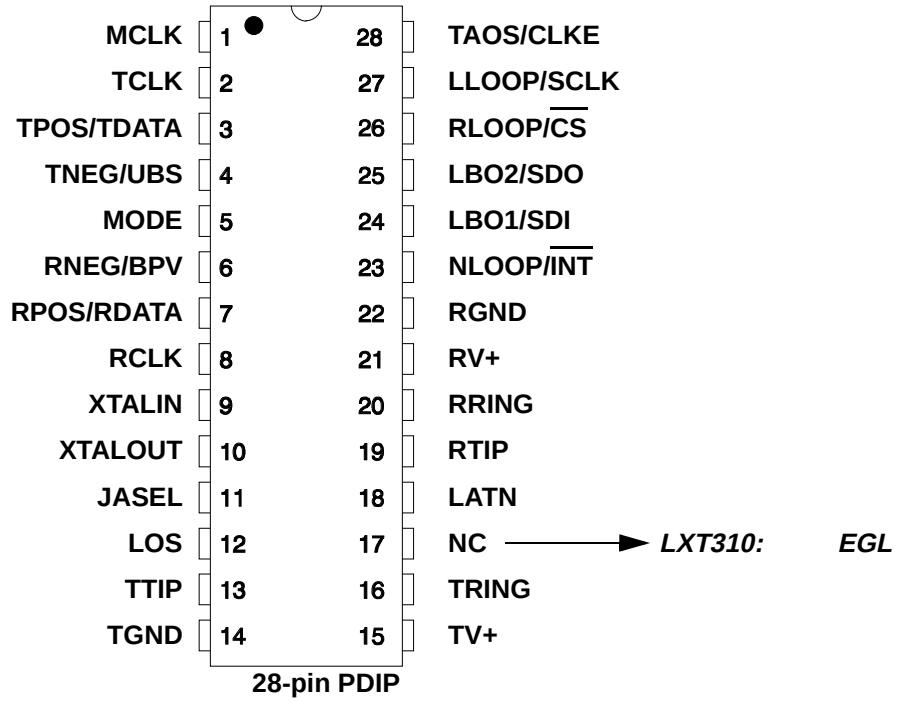
The pinout of the CS61318 differs from that of the LXT318 by one pin, pin 17. The CS61318 data sheet refers to this pin as a "No Connect", while the data sheet for the LXT318 refers to this pin as "GND". This is an acceptable option for pin 17 of the CS61318.



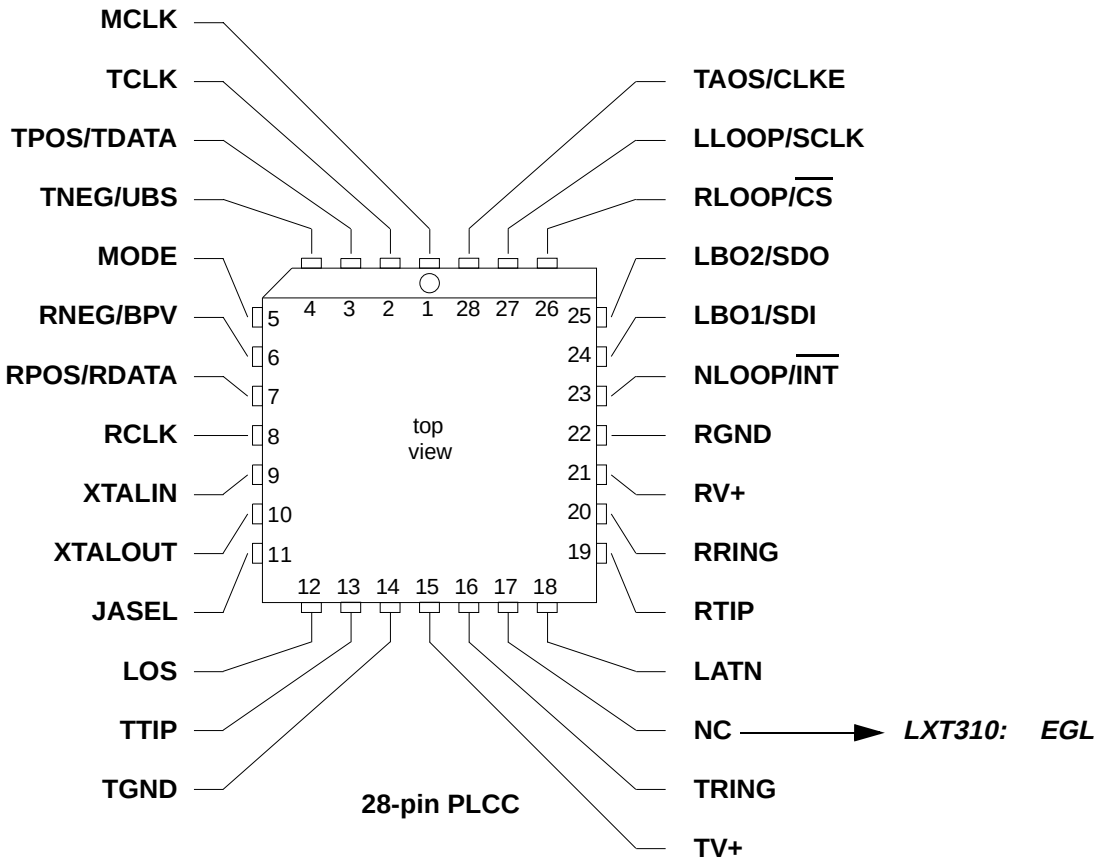
* : LBO Select, LBO1 and LBO2 only available on CS61310.

Figure 1. CS61310/18 Functional Block Diagram

4.2.1 T1 Pinout: CS61310 Shown

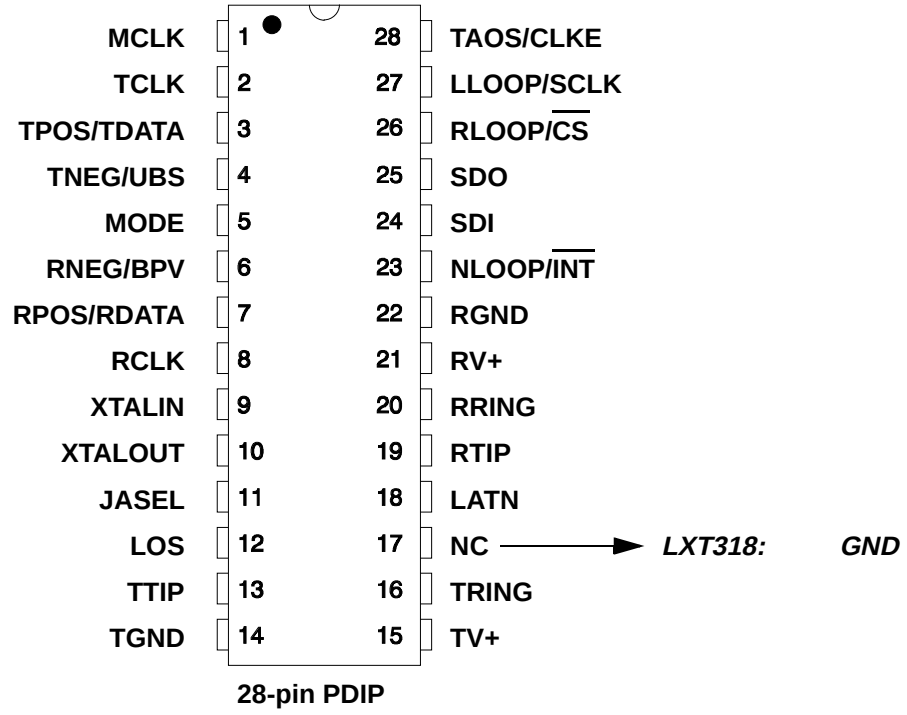


28-pin PDIP

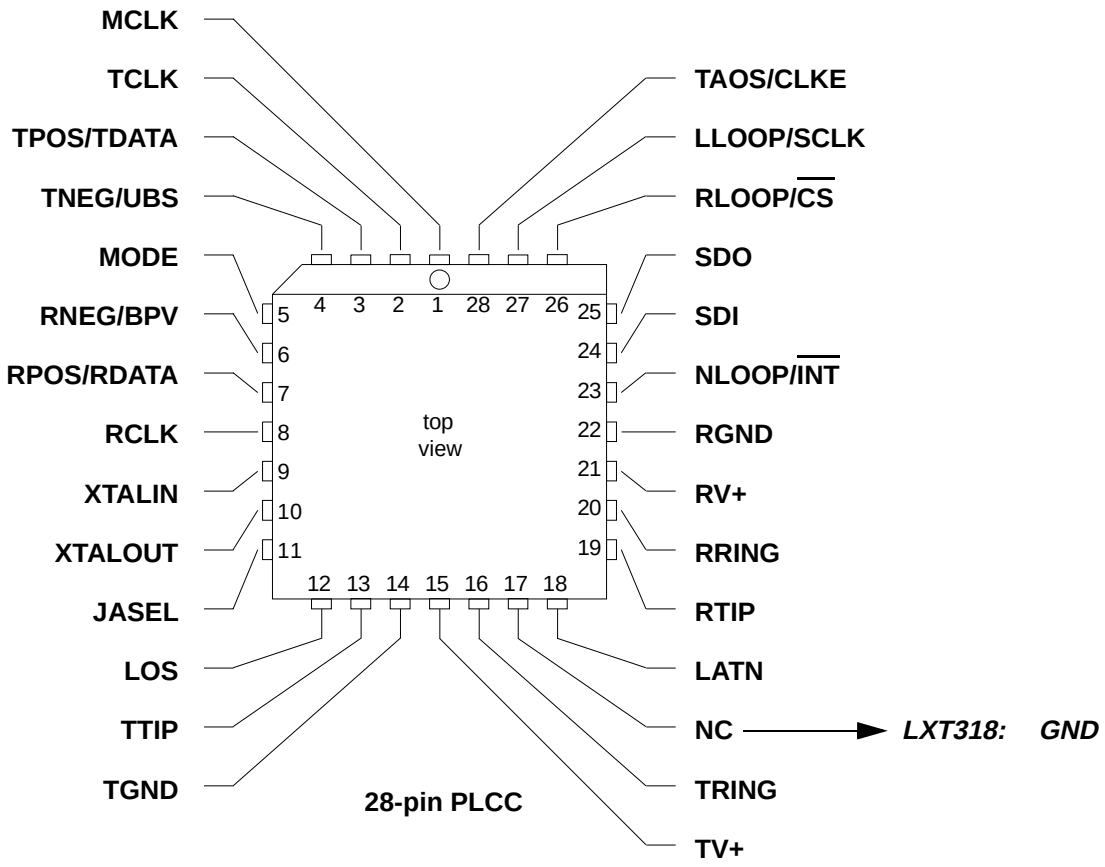


28-pin PLCC

4.2.2 E1 Pinout: CS61318 Shown



28-pin PDIP



28-pin PLCC

4.3 Clocking

The CS61310/18 do not require an external crystal to perform jitter attenuation. Therefore, if the devices are replacing an LXT310/318, the user has three options:

- Retain the pullable crystal required for the Level One circuit, thus making no changes,
- Replace the pullable crystal required for the Level One circuit with a non-pullable crystal, or
- Use no crystal, so long as an external system clock is provided via MCLK.

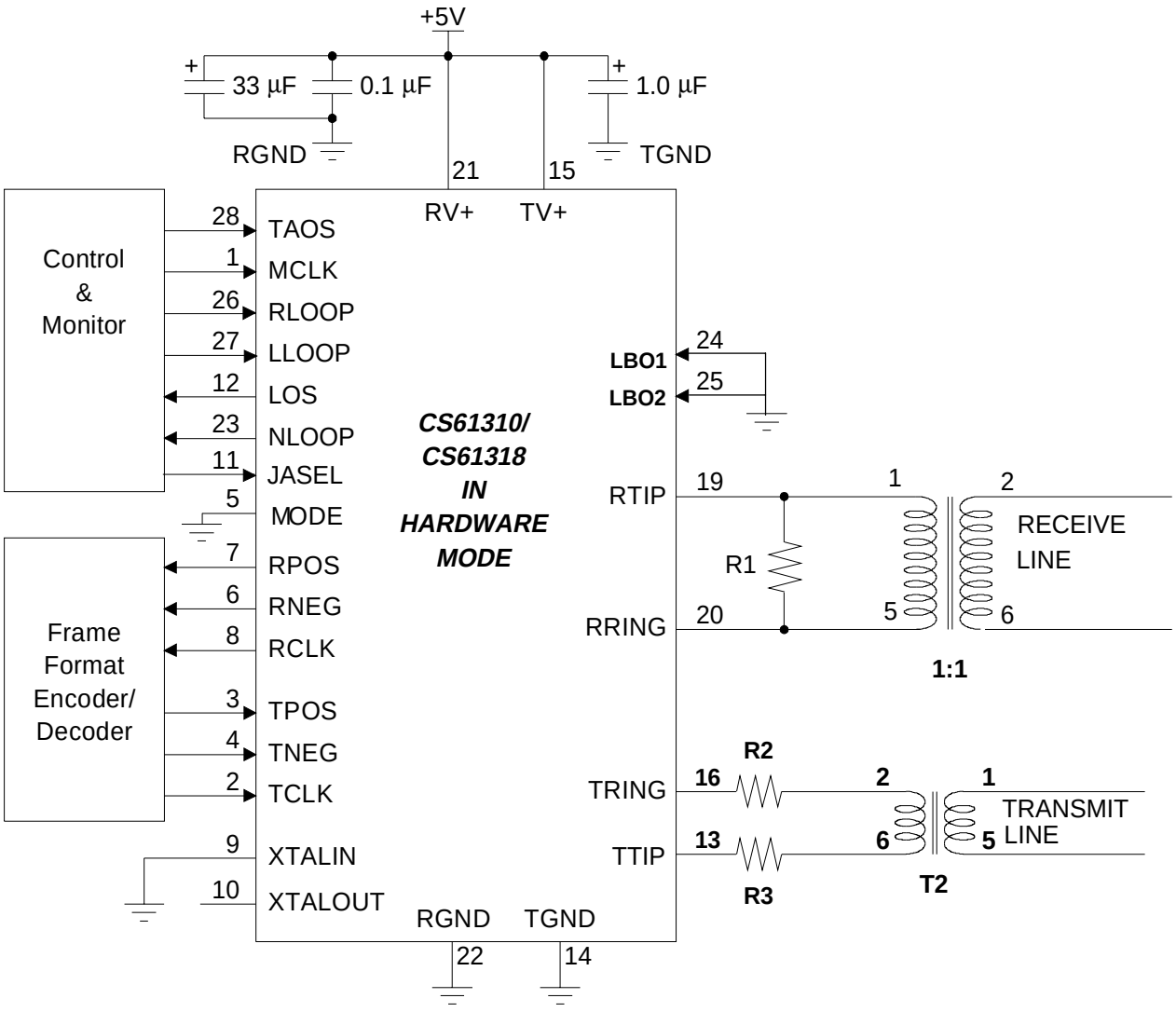
Available Clock Sources	CS61310/CS61318	LXT310/LXT318
Reference provided by external source (through MCLK) only	MCLK at 1X bit rate	MCLK at 1X bit rate
	Drives Receiver and Jitter Attenuator through MCLK	Drives Receiver through MCLK
	External crystal is ignored if transitions detected on MCLK	MCLK actively selected if XTALIN is grounded
	Ground XTALIN to enable Jitter Attenuator	Jitter Attenuator actively disabled if XTALIN pulled up and XTALOUT left open (Note: JA not available if xtal not provided)
	Purity of external clock determines maximum performance of Jitter Attenuator	N/A - Jitter Attenuator not available
	Transmitter driven through TCLK	Transmitter driven through TCLK
Reference provided by external crystal (through XTALIN/OUT) only	Crystal at 4X bit rate	Crystal at 4X bit rate
	Non-pullable	Pullable
	Drives Receiver and Jitter Attenuator through XTALIN, XTALOUT	Drives Receiver and Jitter Attenuator through XTALIN, XTALOUT
	Drive TCLK from external source; can be connected to RCLK	Drive TCLK from external source; can be connected to RCLK
References provided to both MCLK and XTALIN/OUT	Only MCLK will be used	Use external clock to drive Receiver and Transmitter; crystal required to drive Jitter Attenuator

Table 2. Clocking options for the Cirrus and Level One Long Haul LIUs

4.4 Application Modes

4.4.1 Hardware mode

The following layout is a typical hardware-mode application for the CS61310/18.



Note 1: a 0.47µF cap may be necessary on the receive side if common mode noise is an issue.

Note 2: a 0.47µF cap may be necessary on the transmit side to block DC saturation current through T2.

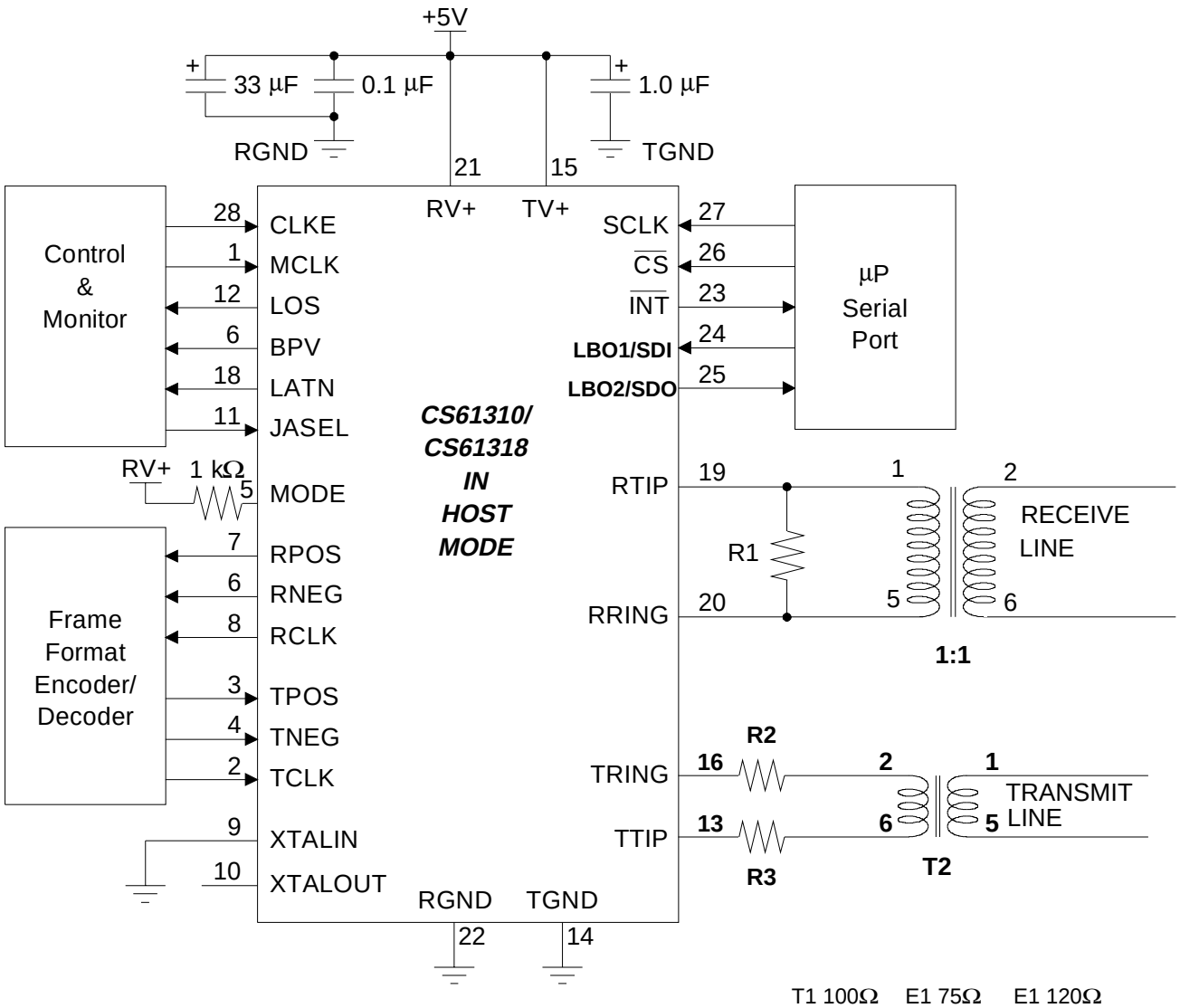
Note 3: When replacing LXT310/318 with CS61310/318, the same crystal may be retained, it may be replaced with a non-pullable crystal, or it may be discarded so long as MCLK is present.

	T1 100Ω	E1 75Ω	E1 120Ω
R1(Ω)	100	75	120
R2(Ω)	9.1	15	15
R3(Ω)	9.1	15	15
T2	1:2	1:1.58	1:2

Figure 2. Typical Hardware-Mode Application for the CS61310/18

4.4.2 Host mode

The following layout is a typical host-mode application for the CS61310/18.



Note 1: a 0.47µF cap may be necessary on the receive side if common mode noise is an issue.

Note 2: a 0.47µF cap may be necessary on the transmit side to block DC saturation current through T2.

Note 3: When replacing LXT310/318 with CS61310/318, the same crystal may be retained, it may be replaced with a non-pullable crystal, or it may be discarded so long as MCLK is present.

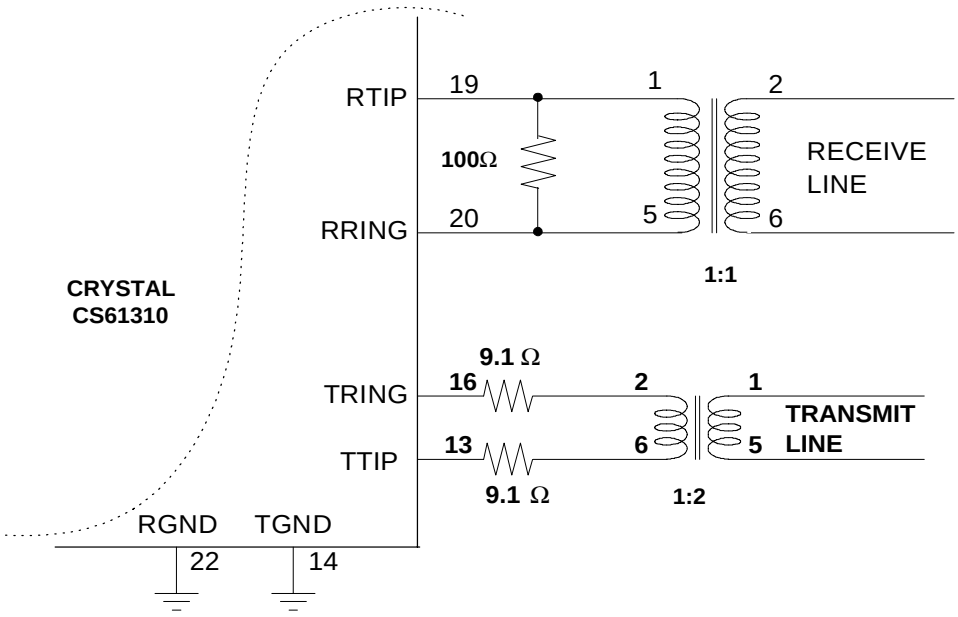
	T1 100Ω	E1 75Ω	E1 120Ω
R1(Ω)	100	75	120
R2(Ω)	9.1	15	15
R3(Ω)	9.1	15	15
T2	1:2	1:1.58	1:2

Figure 3. Typical Host-Mode Application for the CS61310/18

4.5 Layout Comparisons

4.5.1 T1 Layout Comparison: CS61310 versus LXT310

The following partial schematics detail the minor difference in T1 layouts.



Notes:
A 0.47µF capacitor to ground may be necessary on the receive side if common mode noise is an issue. See the CS61310 data sheet.
A 0.47µF capacitor may be necessary in series with one of the transmit matching resistors to block DC saturation current. See the CS61310 data sheet.

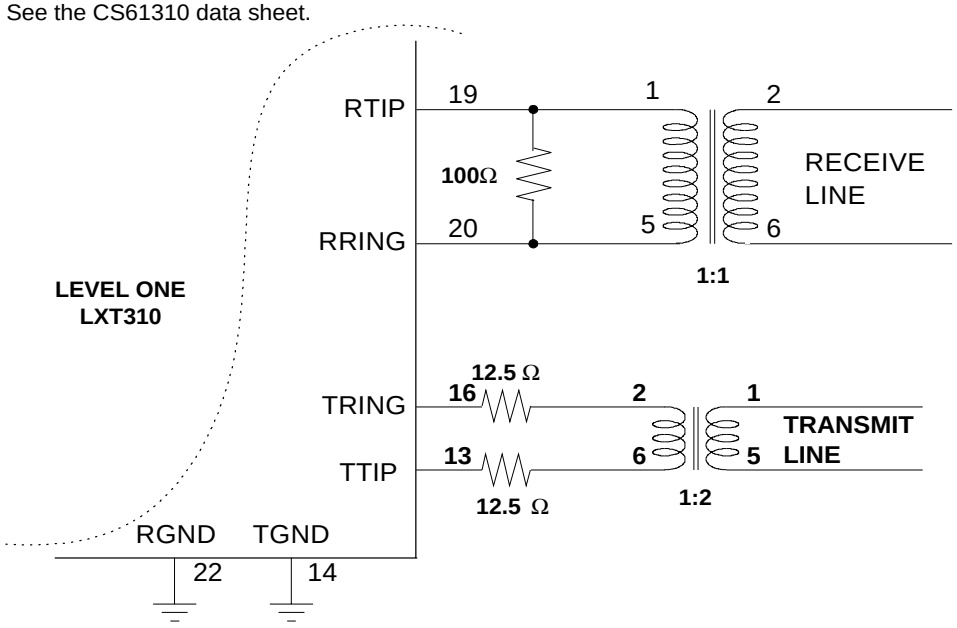


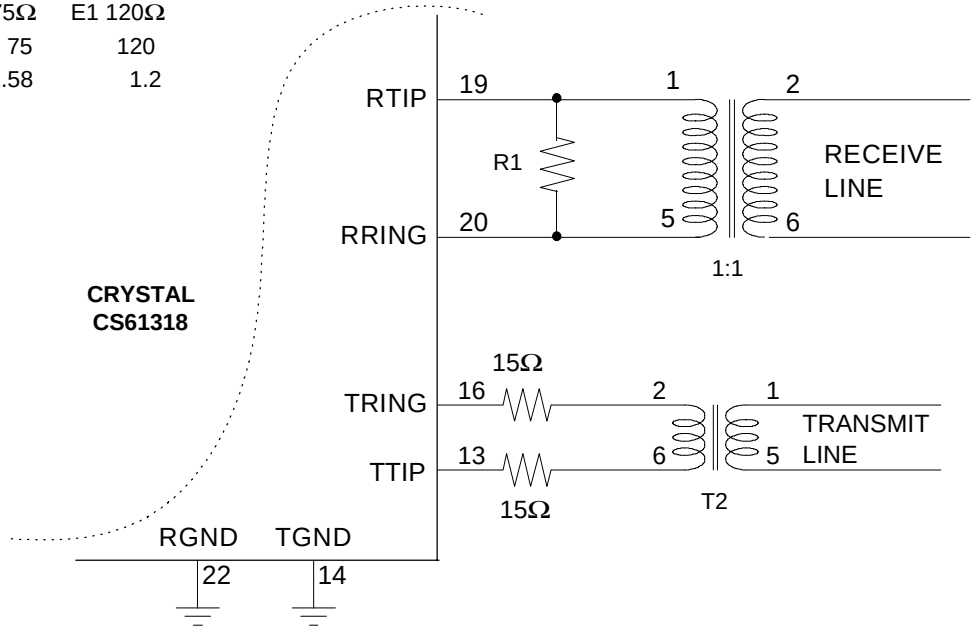
Figure 4. T1 Layout Comparison

4.5.2 E1 Layout Comparison: CS61318 versus LXT318

The following partial schematics emphasize that there are no differences in E1 layout.

Note:

	E1 75Ω	E1 120Ω
R1(Ω)	75	120
T2	1:1.58	1.2



Notes:
A 0.47µF capacitor to ground may be necessary on the receive side if common mode noise is an issue. See the CS61318 data sheet.
A 0.47µF capacitor may be necessary in series with one of the transmit matching resistors to block DC saturation current. See the CS61318 data sheet.

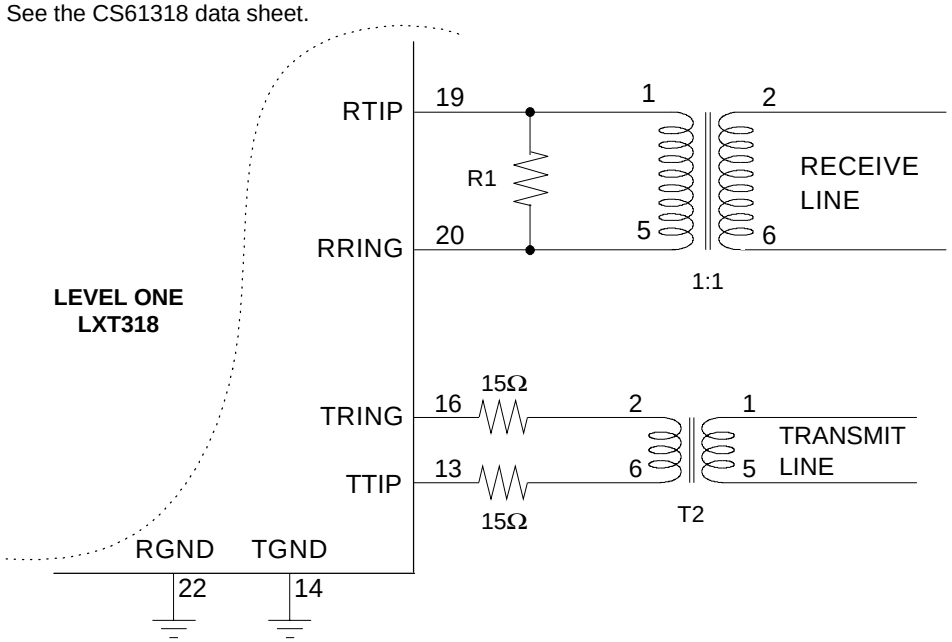


Figure 5. E1 Layout Comparison

4.6 Software Expansion: CS61310/18 shown

The register set of the CS61310/18 is shown below. The Level One equivalent devices provide only a register comparable to CR1 in the CS61310/18. If a user wishes to make use of the additional functionality of the Cirrus Logic devices, it is recommended that the system software be modified to accommodate the additional registers. A complete description of the registers, their functions, and the clock edges upon which serial data is valid may be found in the respective product data sheets.

5. SUMMARY

5.1 Replacing LXT310 with CS61310

- Replace 12.5Ω Transmit resistors with 9.1Ω
- Leave Pin 17 tied to GND, or disconnect
- Keep pullable crystal, replace with non-pullable, or remove
- Enable or disable jitter attenuator per Clocking table
- Implement additional software registers, as desired

5.2 Replacing LXT318 with CS61318

- Leave Pin 17 tied to GND, or disconnect
- Keep pullable crystal, replace with non-pullable, or remove
- Enable or disable jitter attenuator per Clocking table
- Implement additional software registers, as desired

6. CONCLUSION

It is extremely easy to replace the Level One Long Haul LIUs with the Cirrus equivalents. In doing so, users will gain additional functionality (should they wish to make use of it) and will reduce their BOM costs by eliminating the external crystal should they so desire. Design assistance is available from expert engineers at Cirrus Logic. For further information, please contact your local Cirrus representative, call 800-888-5016 or email tcomm@crystal.cirrus.com.

	7	6	5	4	3	2	1	0	ADDR
Control Register 1 (CR1)	TAOS	LLOOP	RLOOP	LBO2[a]	LBO1[b]	CODER TAZ	NLOOP	LOS	0x10 R/W
Control Register 2 (CR2)	AIS	RAMPLSE	RSVD = 0	LOOPDN	LOOPUP	RPWDN	TxHIZ	RSVD = 0	0x11 R/W
Equalizer Gain (EQGAIN)	X	X	X	EQ4	EQ3	EQ2	EQ1	EQ0	0x12 R
RAM Address (RAM)	MSB	-	-	-	-	-	-	LSB	0x13 R/W
Reserved (Set to “0”)	0	0	0	0	0	0	0	0	0x14

Table 3. Control Registers of CS61310/61318

a.Bit 4 of CR1 is reserved (RSVD=0) on the CS61318.
b.Bit 3of CR1 is reserved (RSVD=0) on the CS61318.

• Notes •


SMART
Analog
™